CHAPTER 56

TECHNOLOGY
ELECTRONICS & COMMUNICATION ENGINEERING

Doctoral Theses

01. AGGARWAL (Mona)
Optical Wireless Communication: System Modeling and Performance Analysis.
Supervisor: Prof. Parul Garg
Th 22942

Abstract
(Not Verified)

In this thesis, we study dual-hop relay-assisted OWC system where the two distant nodes communicate with the help of a single relay. The relaying techniques help in mitigating the adverse effects of channel conditions as well as to enhance the coverage area. Throughout this research work we consider subcarrier intensity modulation (SIM) based M-ary constellations. Under the combined influence of atmospheric turbulence, path loss and pointing errors, all the channels are modeled by independent but not necessarily identically distributed (i.n.i.d.) Gamma-Gamma fading statistics. In this thesis, we first focus on the SIM-based decode and forward (DF) relayed OWC systems. Next, the performance of SIM based variable gain amplify and forward (AF) relayed OWC systems is investigated with the assumption that the channel state information (CSI) is available at the communicating terminals. The equivalent end-to-end SNR of the system is upper bounded with the help of harmonic-geometric mean (HGM) inequality and the performance of the system is analyzed under various channel adaptive transmission schemes. We evaluate closed form expressions for channel capacity under these transmission schemes and compare them. Further, we use the moment generating function (MGF) based approach to obtain the exact analytical framework for AF relayed OWC systems. The exact analysis is carried out for both types of AF relays i.e. variable-gain and fixed-gain under the umbrella of special functions such as Meijer's G-function and bivariate Meijer's G-function (BMGF). Finally, we propose hybrid decode-amplify-forward (DAF) relaying scheme for relay assisted OWC systems where the relay can adaptively switch between AF and DF mode.

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02. IYER (Sridhar)
Some Studies on Impact of Physical Layer Impairments (PLIs) on the Performance of Optical WDM Networks.
Supervisor: Dr. Shree Prakash Singh
Th 22943

Abstract
(Not Verified)

We address the PLI-RWA, RP, WCP, latency awareness and OCP issues in translucent WDM networks. We introduce an innovative PLISQARWA algorithm which evaluates candidate routes that demonstrate highest signal quality. The QoT of optical signal is evaluated through Q-factor which is computed by means of a mathematical model that accounts for simultaneous impact of four dominant PLIs namely, SRS, FWM, XPM, ASE noise. Further, we also show that by equipping routing phase of PLI-SQARWA with delay awareness, zero blocking is achievable. We propose a hybrid translucent node architecture that is an electro-optical solution for reducing the time delay due to OEO conversions. We show that, in comparison to the translucent and transparent node architectures present in literature, which employ OEO conversions for both, regeneration and/or wavelength conversion, the hybrid node demonstrates lower optimum delay and incurs lesser time delay, at a similar blocking performance. Further, in order to control operations of the hybrid translucent node, we propose an OCP approach which disseminates information about network components to all the network nodes. We show that compared to a recently proposed hybrid OCP approach, the proposed OCP methodology demonstrates lower connection blocking and minimizes the overall network cost, while demonstrating acceptable lightpath establishment setup times at all traffic loads. Finally, results highlight the significance of equipping the routing phase of a PLI-RWA algorithm with signal quality and delay awareness and suggest that for OEO conversion generated time delay minimization, using AOWCs for only wavelength contention resolution is a judicious choice rather than resorting to regenerators and further, there exists a definitive trade-off between the overall network cost and maximum tolerable delay.

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03. MANJEET KUMAR
Design of Fractional-Order and Fractional –Delay Digital Filters.
Supervisor: Dr. Tarun Kumar Rawat
Th 23197

Abstract
(Verified)

Fractional calculus has maintained tremendous vitality in various area of image processing, automatic control systems, robotics, signal processing, circuit theory and biomedical engineering. It involves a unique feature of generalization of integral and derivative to a non-integer orders. The enormous growth has been observed in the past few decades, which revolutionise the field of fractional-order differentiators (FOD) and fractional-delay (FD) filters design. Over the past couple of decades different methods have been developed based on discretization techniques, interpolation techniques and approximation techniques for the design of FOD and FD filters with great accuracy. This thesis is an attempt made by the authors to design optimal fractional order digital differentiator and fractional delay filters. This work presents the designing of fractional-order differentiator using least squares method that is used to compute the fractional derivative of the power function. The proposed design shows the superior performance over the existing method in the higher frequency region of the frequency response of the designed FOD. Evolutionary algorithms like cuckoo search algorithm (CSA) and genetic algorithm (GA) are used to design optimal FIR fractional order differentiator. The proposed FIR-FOD design using CSA and GA have been proved to be very robust, simple and generic. The effectiveness of the proposed methods is evaluated and compared with the existing interpolation based methods. This thesis also focuses on the design of fractional-delay infinite impulse response (FD-IIR) filter using nature inspired algorithms. Here, three nature inspired algorithms, namely genetic algorithm, particle swarm optimization (PSO) and the cuckoo search algorithm are employed to determine the optimal coefficients of FD-IIR filters.

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1. Introduction. 2. Fractional order digital differentiator design based on power function and least-squares 3. Optimal design of FIR fractional order differentiator 4. Optimal fractional delay-IIR filter design 5. Conclusions and suggestions for future work.

04. SHARMA (Nikhil)
Design and Analysis of Free Space Optical and Asymmetric RF/FSO Communication Systems.
Supervisor: Prof. Parul Garg
Th 23198

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1. Introduction 2. Selective DF relaying based FSO system with generalized turbulence 3. Spectrally efficient TWR assisted FSO communication with generalized pointing error 4. Bi-directional symmetric RF/FSO system with η - μ/ gamma-gamma fading distribution 5. Relay selection in asymmetric RF/FSO system 6. Low complexity decoding in dual relay assisted asymmetric RF/FSO system 7. Generalized orthogonal space-time block code based MIMO FSO system 8. Conclusion and future work. Publications based on this thesis. Biodata of the author. Bibliography.

05. PANDA (Jeebananda)
Study of Watermarking Techniques for Digital Data.
Supervisor: Prof. Asok Bhattacharyya
Th 22944

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1. Introduction. 2. Watermarking of Image. 3. Watermarking of video. 4. Watermarking of audio. 5. Watermarking of text. 6. Watermarking of sequential circuit design. 7. Conclusions. References, list of publications and biodata of author.

06. RAI (Shireesh Kumar)
Analysis and Design of Analog VLSI Circuits.
Supervisor: Prof. Maneesha Gupta
Th 22945

Abstract
(Verified)

Current mode analog signal processing is gaining popularity from past few decades due to its attractive advantages offered under certain conditions as compared to their voltage mode counterparts. These advantages are larger dynamic range, wider bandwidth and less power dissipations. The transistors used in current mode devices exploit the maximum unity gain bandwidth (f_T) which results in higher bandwidth. The advantages of current mode devices and recent developments have led to many new current mode analog building blocks. These building blocks are enjoying the latest techniques involved in the circuit designing while preserve the earlier concepts used in the design of analog circuits. One such current mode analog building block which has attracted many researchers is current differencing transconductance amplifier (CDTA). It is now widely being used in several applications of analog signal processing. It has been observed in literature that CDTA offers limited range of transconductance. The center frequency (f_0) of filters and frequency of oscillation (f_0) of oscillators both depend on transconductance (g_m) of CDTA. The limited range of transconductance restricts the use of CDTA in high frequency applications though the bandwidth is very high. Thus, a high and wide range of transconductance (g_m) is required in order to utilize

the block in high frequency applications. In the thesis, the transconductance of CDTA has been enhanced by applying various gm boosting techniques. Generally, the transconductance of CDTA has been enhanced by increasing the biasing current of differential pair which often results in higher power dissipation and limited range of transconductance. The enhancement in the transconductance is also obtained by increasing the size of transistors of differential pair which limits the linear range of CDTA. The disadvantages of both the techniques have been overcome by some novel techniques of gm boosting proposed in different chapters of the thesis.

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07. TIWARI (Satish Chandra)
Low Power High Density Flip-Flops and their Applications.
Supervisor: Dr. Maneesha Gupta
Th 22946

Abstract
(Not Verified)

In this modern era where IOT's and hendheld devices are gaining importance, there is a need to develop new generation SoCs which are faster, power efficient as well as cheap as compared to their processors. FFs (FFs) plays very important role in realizing SoCs and they are vital in terms of frequency of operation as well as power dissipation of system. FF and latches account for 30-70% of the total chip power dissipation in digital systems. With technology shrinking to more advanced nodes, there is a need for FFs with low power consumption and robust operation at low voltages. This work presents three new FF architectures along with their characterizations. Two single edge triggered FF configurations have been proposed while the third one is a low power double edge triggered FF. From an application perspective of the proposed FFs, synchronizers and counters have been explicitly discussed. Application of the proposed Flip-Flops have been studied for few of the circuits. In addition, standard algorithms are developed for characterizing different parameters of FFs. Two novel fully automated algorithms are developed to characterize driving strength of FF (FF) or any digital circuit. One of the algorithm makes use of Levenberg-Marquardt method and the other algorithm uses Logical Effort (LE) theory for transistor width characterizations. These algorithms are capable of characterizing not only FF circuit but any CMOS digital circuit for a given capacitive load. It is well known that any improvement at the transistor level has a huge impact on the overall performance of any digital/analog system. Since FGMOS has low voltage operating characteristics, this work has analyzed it as an alternative of the MOS transistors. This work also introduces a novel methodology for the estimation of optimum gate capacitance value of N-input FGMOS under any technology.

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